15-Watt Internally Matched GaAs FETs and 20-Watt Amplifier Operating at 6 GHz

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Abstract

6-GHz 15-Watt and 8-GHz 10-Watt internally matched GaAs FETs have been developed. The lumped-element two section input matching network is formed on ceramic plates with a high dielectric constant. The distributed single section output circuit is formed in microstrip pattern on an alumina plate. A 6-GHz 20-Watt balanced amplifier module has been realized using the internally matched devices which operate without any external matching.

Introduction

High power GaAs FETs, exhibiting significant progress in recent years, are realized basically by increasing the total gate width as well as the drain-source breakdown voltage. As a result, device input and output impedances decrease and the device width increases steadily, in proportion to the total gate width. These give rise to a serious problem of uniform and low-loss matching. To solve such matching limitation and exhibit the basic device capabilities, the introduction of an internally matched form is a natural consequence. Efforts have been made toward developing the internal matching networks for high-power GaAs FETs.[1][2][4]

This paper presents further improvement of GaAs FET's performance obtained by developing the advanced internal matching technique on multi-chip devices and by improving the basic FET structure. The developed internally matched FETs delivered 15-Watt at 6-GHz and 10-Watt at 8-GHz without any external matching. A 20-Watt 6-HGz balanced amplifier module was realized using the internally matched devices.

Matching Network Design and Description

The GaAs MES FET has a graded recess structure, which was adopted to decrease source resistance without degrading drain breakdown voltage. The single-chip GaAs MES FET has a six-cell structure consisting of 84 parallel-gates with six gate bonding pads and six drain pads. Gate length is 1.3μm and total gate width of the single-chip FET is 8.4mm. The single-chip measures 2.25x0.65mm. The real part of the single-chip FET input impedance is nearly 1Ω. To reduce bonding wire inductance for source grounding, the source electrode is grounded by thin metal films evaporated on the device periphery.

The equivalent circuit of the internal matching network is shown in Fig.1. Input internal matching networks of lumped-element two-section low pass type and output matching networks of one section semi-distributed form, were designed. Based on small-signal S-parameters, a computer-aided design optimization was performed, where large-signal matching was attemped by considering the increase in the optimum power load conductance of the FETs with the increase in input power drive level. Then, with the equivalent load-pull measurements,[3] the output internal matching networks were experimentally optimized to obtain high-power output over the design frequency range. Four-chip 33.6mm gate-width FETs were internally matched over the 5.6-6.4GHz and 7.6-8.1 GHz ranges, and two-chip 16.8mm gate-width FETs were internally matched over the 5.7-6.5GHz range.

A photograph of four-chip GaAs FET (33.6mm total gate width) with the internal matching network is shown in Fig.2. The input matching network of lumped elements consists of parallel capacitors on two ceramic plates, 0.1mm thick (relative dielectric constant ε_r=39) and 30μm diameter Au bonding wires. By the introduction of the so called tree structure, as shown in Fig.2, input phase uniformity within multicell and multichip devices was achieved. The output circuit consists of bonding wires and parallel microstrip stubs formed on a 1mm -thick alumina ceramic substrate. Input and output terminals are composed of 50Ω microstrip lines.

Performance

The small-signal output impedance and large-signal optimum power load impedance Z_{LO} of the 6-GHz 16.8mm gate-width FET with the internal matching network are shown in Fig.3. In the figure, the circles show small-signal impedances and the filled circles show optimum power load impedances. The small-signal optimum power load impedance (A:18.6dBm IN at 6.2GHz) is the complex conjugate of the small-signal output impedance. And the higher input drive level becomes, the closer to 50Ω the optimum power load impedance becomes.

As shown in Figs.4 and 5, the 6-GHz 33.6mm gate-width device has a 12-W power output at 1-dB gain compression and a 15-W saturated power output and 26.8% maximum power added efficiency with a linear gain of 6.4±0.6dB from5.6 to 6.4 GHz range. The 8-GHz 33.6mm-device has an 8-W power output at 1-dB gain compression and 10.5-W saturated power output and 11.2% maximum power added efficiency with a linear gain of 4.5±0.5dB from 7.6 to 8.1GHz range. As the single chip (8.4mm gate width) has a 4-W saturated output power at 6 GHz, the performance was achieved with a power combining efficiency of 94%. In the figures, the characteristics of a 6-GHz 16.8mm gate-width device is also described. The 16.8mm-device has a 7.9-W saturated power output and 27% maximum power added efficiency with a

linear gain of 5.8±1dB from 5.8 to 6.5 GHz range.

Fig.6 shows distortion characteristics of the 16.8mm device. 3rd-order intermodulation distortion (IMD3) calculated from AM-AM and AM-PM conversion characteristics, and IMD3 measured by injecting two equal amplitude signals separated in frequency by 10 MHz are shown in the figure. The calculated IMD3 fits in well with the measured IMD3.

Balanced Amplifier module

The developed balanced amplifier module consists of two 33.6mm gate width devices and two 16.8mm gate width devices. As shown in Fig.7, a 16.8mm-device and a 33.6mm-device are cascaded directly. Two cascaded amplifiers are combined by two 3dB branch type microstrip hybrids. Each internally matched device needs no external matching network to construct cascaded amplifiers. The hybrids and transmission lines are formed on 0.6mm-thick teflon glass fiber substrates (ε_r=2.6). The balanced amplifier module has a 17-W power output at 1-dB gain compression and 22.4-W saturated output power and 15.7% maximum power added efficiency with a linear gain of 9±1.3dB from 5.7 to 6.3 GHz, as shown in Figs. 8 and 9.

Conclusion

6-GHz 15-Watt and 8-GHz 10-Watt internally matched GaAs FETs have been developed. A 6-GHz 20-Watt balanced amplifier module has been realized using the internally matched devices which operate without any external matching.

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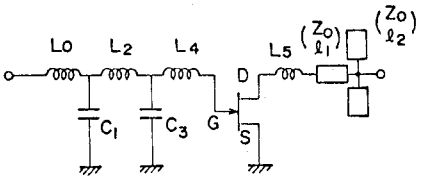

Fig.1 Equivalent circuit of internally matched GaAs MESFET

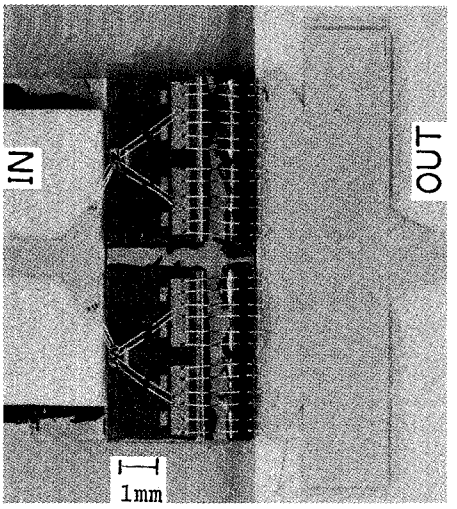

Fig.2 Internally matched FET with 33.6mm total gate width (6-GHz)

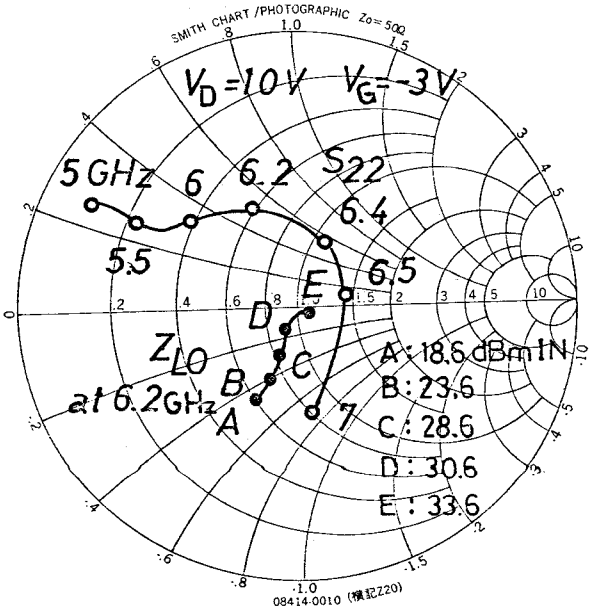

Fig.3 Small-signal output impedance and large-signal optimum power load impedance of 6-GHz 16.8mm gate-width FET with internal matching network.

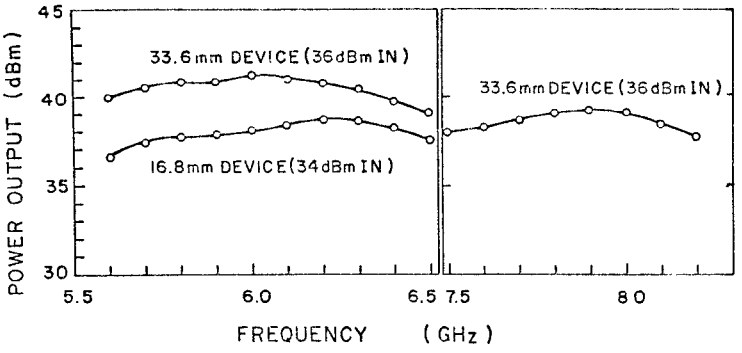

Fig.4 Output power response versus frequency of internally matched FETs , measured without any external matching.

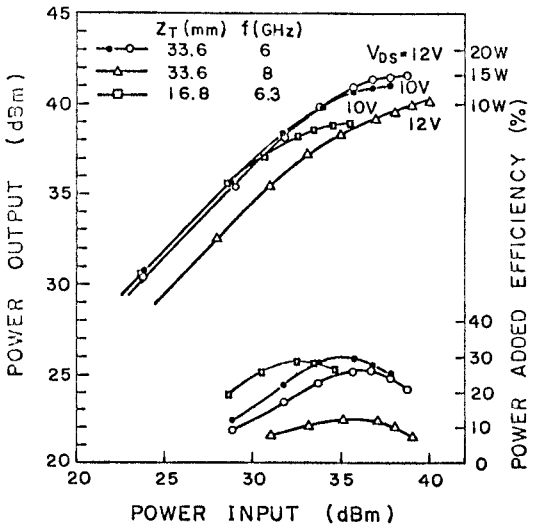

Fig.5 Input-output response of internally matched FETs , measured without any external matching.

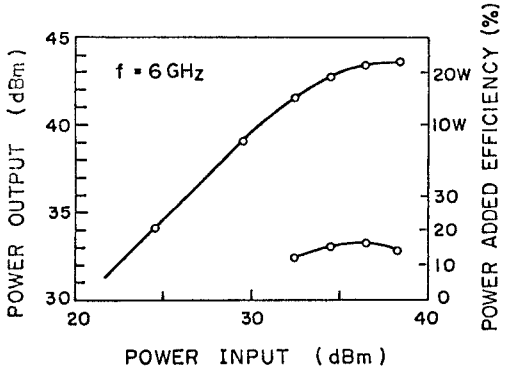

Fig.8 Input-output response of balanced amplifier module.

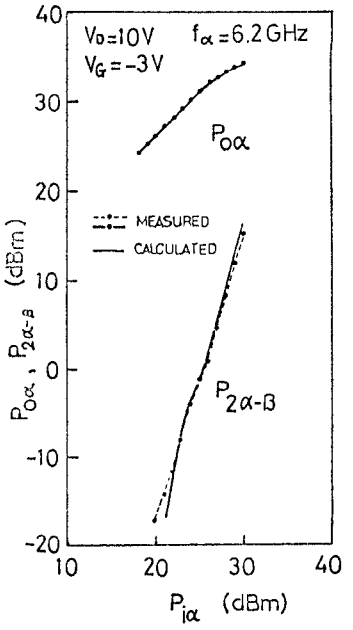

Fig.6 Calculated values and measured values of 3rd-order IMD. (6-GHz 16.8mm gate-width device)

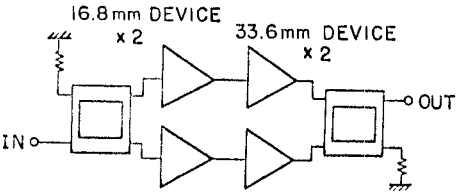

Fig.7 Circuit configuration of a balanced amplifier module.

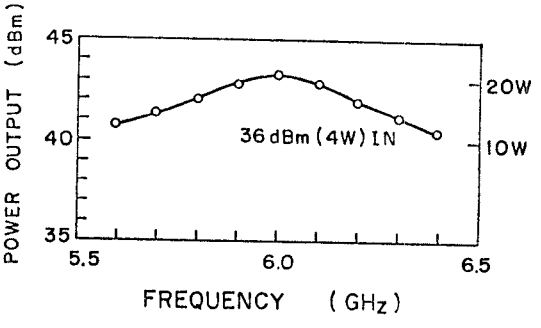

Fig.9 Output power response versus frequency of balanced amplifier module.